

WHAT IS CLAIMED IS:

1. A memory cell array, comprising:
 - 5 a plurality of magnetic cell junctions; and
 - a first conductive line comprising:
 - 10 a gate of a first transistor configured to enable a read operation for one of the plurality of magnetic cell junctions; and
 - a gate of a second transistor configured to enable a write operation for another of the plurality of magnetic cell junctions.
- 15 2. The memory cell array of claim 1, wherein the gate of the first transistor is one of a plurality of gates within the first conductive line configured to enable read operations for a first set of the magnetic cell junctions and wherein the gate of the second transistor is one of a plurality of gates within the first conductive line configured to enable write operations for a second set of the magnetic cell junctions.
- 20 3. The memory cell array of claim 2, wherein the gates configured to enable read operations for the first set of the magnetic cell junctions and the gates configured to enable write operations for the second set of the magnetic cell junctions are alternately arranged within the first conductive line.
- 25 4. The memory cell array of claim 1, further comprising a second conductive line comprising:
 - 30 a gate of a third transistor configured to enable a write operation for the magnetic cell junction having a read operation enabled by the first transistor; and
 - a gate of a fourth transistor configured to enable a read operation for the magnetic cell junction having a write operation enabled by the second transistor.

5. The memory cell array of claim 4, wherein the second and third transistors are coupled to a common program line.
6. The memory cell array of claim 4, wherein the first and fourth transistors are coupled to a common ground contact.
7. The memory cell array of claim 4, wherein the first and second conductive lines are coupled to a common word line.
8. A memory cell array, comprising:
- a magnetic cell junction;
 - a bit line spaced apart from the magnetic cell junction;
 - a first set of conductive structures serially coupled to the bit line, wherein one or more of the first set of conductive structures are configured to induce a magnetic field about the magnetic cell junction;
 - a transistor coupled to the first set of conductive structures; and
 - a program line collectively configured with the bit line to induce current flow through the first set of conductive structures upon an application of a voltage to a gate of the transistor.
9. The memory cell array of claim 8, wherein the program line is further configured, with a different bit line, to induce current flow through a second set of conductive structures arranged adjacent to a different magnetic cell junction of the array upon an application of a voltage to a gate of a different transistor.

10. The memory cell array of claim 8, wherein the first set of conductive structures comprises at least two segments respectively aligned with opposing sides of the magnetic cell junction.
- 5 11. The memory cell array of claim 10, wherein the first set of conductive structures comprises a third segment connecting the at least two segments.
12. The memory cell array of claim 10, wherein the at least two segments are arranged parallel to each other.
- 10 13. The memory cell array of claim 12, wherein the magnetic cell junction is configured to have an easy axis arranged at an angle between approximately 0° and approximately 90° relative to the two segments.
- 15 14. The memory cell array of claim 10, wherein at least one of the two segments is arranged in contact with the magnetic cell junction.
15. The memory cell array of claim 10, wherein at least one of the two segments is electrically connected to the magnetic cell junction through a via.
- 20 16. The memory cell array of claim 7, wherein the bit line is spaced directly above the magnetic cell junction.
17. A memory array, comprising:
- 25 a plurality of magnetic cell junctions;
- a bit line spaced above and arranged in vertical alignment with the plurality of magnetic cell junctions; and
- 30 a series one or more conductive structures coupled between the bit line and one of the plurality of magnetic cell junctions.

18. The memory array of claim 17, wherein the series of one or more conductive structures is configured to induce a magnetic field about the magnetic cell junction.

19. The memory array of claim 17, further comprising:

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a transistor coupled to the series of one or more conductive structures; and

a program line collectively configured with the bit line to induce current flow
through the series of one or more conductive structures upon an
10 application of voltage to a gate of the transistor.

20. The memory array of claim 17, wherein the series of one or more conductive structures is one of a plurality of sets of serially connected conductive structures coupled between the bit line and the plurality of magnetic cell junctions.

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